Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.033”**

**P**

**.033”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GATE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .033” X .033” DATE: 12/3/20**

**MFG: CRYSTALONICS THICKNESS .000” P/N: 2N5115**

**DG 10.1.2**

#### Rev B, 7/1